Paul Nieves

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EDUCATION

Rensselaer Polytechnic Institute | Troy, NY — **May 2024 - May 2025**
M.S. Electrical Engineering (Concentration: Computer Systems Design) — **GPA:** 3.51
Rensselaer Polytechnic Institute | Troy, NY — **May 2020 - May 2024**
B.S. Electrical and Computer Systems Engineering Dual — **GPA:** 3.48

EXPERIENCE

Collins Aerospace | Aguadilla, PR — **May 2025 – Present**
FPGA Engineer

- Support the Mission Systems (MiS) team on the Terminal High Altitude Area Defense (THAAD) program by delivering customer documentation—including AS051, AS057, TEC memos, Test Plans, and PCN/SRI Reports—to Lockheed Martin.
- Developed a Python automation app to apply Controlled Unclassified Information (CUI) markings across multiple document types, streamlining documentation workflows, improving compliance, and saving 56 hours per employee annually.
- Delivered a presentation on FPGA/ASIC fundamentals to support team learning and contribute my background in the area.
- Created a Power Apps solution to monitor task progress and delivery timeliness, while facilitating document approval and release workflows.

Claro Puerto Rico | Guaynabo, PR — **May 2024 – Aug 2024**
Network Technician

- Maintained demarcation points for residential and commercial clients (Demarcation points: Tmarc, ASR 9k/920, Cisco 3000)
- Diagnosed and resolved signal loss and connectivity issues for fiber optics, copper, and coaxial networks

Green Action Studio | Schenectady, NY — **Sep 2022 – Dec 2022**
Embedded Hardware Engineer

- Engineered PCB modules for an electric vehicle charger and designed a UL-approved ground fault detection circuit.
- Verified ARM-based microcontroller firmware and assembled EV chargers from schematics

PROJECTS

Multilevel Cache Coherence | Troy, NY
ECSE 6700 – Advanced Computer Hardware Design

- Developed a multi-core MESI-based cache coherence system integrating RAM, set-associative caches, and an arbiter
- Validated Verilog code reliability via comprehensive simulation test vectors and waveform analysis

Variable IIR and FIR Filters | Troy, NY
ECSE 6680 – Advanced VLSI Design

- Implemented a variable pipelined IIR filter in SystemVerilog for audio equalization and reduced critical path of the system
- Designed a 102-tap low-pass FIR filter using parallel processing (L=2/L=3), achieving >80 dB stopband attenuation

Pipelined RISC-V Processor | Troy, NY
ECSE 4770 - Computer Hardware Design

- Designed a 5-stage pipelined processor supporting key RISC-V instructions with hazard detection
- Verified functionality through SystemVerilog testbench, RTL schematics, and waveform analysis

FPGA UART Core | San Juan, PR
Personal Project – Verilog, Serial Comms, Testbench

- Designed a parameterized UART TX/RX core in SystemVerilog with baud-rate generation and FIFO buffering.
- Verified functionality using testbenches and waveform-based timing analysis.
- Deployed and tested on FPGA hardware to validate reliable serial communication.

PDF Editing Automation Builder Application | Aguadilla, PR
Personal Project - React, Electron, JavaScript, Python, HTML/CSS

- Built an **electron desktop application** automating PDF workflows with a block-based builder, reducing repetitive tasks.
- Connected **React frontend** to Python PDF processing via **Electron IPC**, enabling configurable, local execution with persistent state.

Home Media & File Server Application | Aguadilla, PR
Personal Project - Docker, Linux, Nginx, Media/File Servers

- Built and deployed a **Linux-based server** using **Docker Compose** to host Immich, Jellyfin, and Seafile for media streaming and file management.

CIFAR-10 Image Classification Using Convolutional Neural Networks | Troy, NY
ECSE 6965 – Reinforcement learning, PyTorch API

- Designed and trained a **CNN** achieving **94.64% accuracy** on CIFAR-10 with **4.59M parameters** using data augmentation.

Static CMOS Logic Design & Layout for VLSI (65 nm) | Troy, NY
ECSE 4220 – VLSI Design

- Optimized a CMOS circuit using Karnaugh maps, minimizing transistor count for efficiency
- Developed a compact, DRC-compliant layout with minimal interconnects
- Verified through Layout vs. Schematic (LVS) and performed parasitic extraction (PEX)

Deep Q-Learning for CartPole Control Problem | Troy, NY
ECSE 6965 – Reinforcement Learning

- Implemented a Deep Q-Network (DQN) to balance a pole using reinforcement learning
- Designed a neural network from scratch with experience replay and a target network for stable learning
- Tuned hyperparameters, achieving an average reward of 200 over 100 episodes

Modular Synth | Troy, NY
ECSE 6980 - Masters Project

- Designed PCBs for VCO, VCA, MIDI-to-CV, ADSR, and a ±15V/±20V DC power supply for a modular synthesizer
- Programmed firmware for Arduino Nano (ARM) to interface with 16-bit DACs through SPI for 1mV precision analog note

Drone | San Juan, PR
Personal Project – Soldering, Embedded Control

- Built a drone that can record and provide a live feed to a small monitor.

Personal Portfolio Website | Troy, NY
Personal Project - JavaScript, HTML/CSS, REST APIs

- Built and deployed a full-stack portfolio website with a RESTful backend endpoint to handle contact form submissions.
- Implemented input validation, JSON-based request handling, and error management for reliable client-server communication.
- Integrated frontend and backend using asynchronous HTTP requests and POST-based workflows.

RESEARCH

LESA Florescence Tool Research | Troy, NY **Sep 2023 – Dec 2023**
Software Engineer/Embedded Hardware Engineer

- Built, integrated, and tested Fluorescence tool hardware for plant health analysis
- Debugged and enhanced Lock-in Amplifier Circuit by adding filters to better detect fluorescence wavelength from plants

Photonics GUI Research | Troy, NY **Sep 2023 – Dec 2023**
Software Engineer/Embedded Hardware Engineer

- Automated Tektronix oscilloscope, multimeter, and function generator with Python via GPIB (py-visa)
- Developed a GUI for streamlined test execution and result storage. (Integrated cloud saving into GUI)

SKILLS

Programming: C#, C++, C, Python, Java, React js, SystemVerilog, MIPS, VHDL, Power Bi
Hardware Design: PCB (Altium, KiCAD, EAGLE), FPGA, VLSI Layout, SPI, UART, I2C, JTAG, oscilloscopes, logic analyzers
Software & Tools: Git, MATLAB, Quartus Prime, Vivado, ModelSim, Cadence, LTSpice, Arduino IDE, Synopsys Design Compiler
Languages: Fluent in English & Spanish

LICENSES

Amateur Radio Operator Class License - Federal Communications Commission **Issued May 2023 – Expires May 2033**

- Credential ID KE2BLP